64.(Amended) The integrated circuit of claim 63 where the layer is planar within a thickness variation of about 20%.

65.(Amended) An integrated circuit, comprising:

a substrate of a first material;

an insulator of a second material overlying the substrate;

a multiple contact hole[s] through the insulator to the substrate,[ each] the contact hole having at least one sidewall of the second material and a separate generally planar layer of a silicide contacting only the substrate.

## REMARKS

Applicant has considered the Office Action mailed on October 26, 2001, and the references cited therewith. Claim 38 is canceled and claims 31, 39, 43, 48, 55, 59, and 63-65 are amended, so that claims 31-37 and 39-70 remain pending in this application.

## §112 Rejections

Claims 63 and 64 were rejected under 35 USC § 112, first paragraph. These claims have been amended to incorporate the "thickness variation" terminology used in the Specification at page 12 lines 1-6 and page 14 lines 20-24.

Claim 38 was rejected under 35 USC § 112, second paragraph, as indefinite. This claim has been cancelled.

The Drawing was objected to as not showing the multiple contact holes recited in claims 59 and 65. These claims were amended to recite "a contact hole" in an integrated circuit. These changes do not narrow the scope of the claims, because of the well-settled doctrine that a claim reciting "a(n)" element is infringed by a device having more than one of that element.

## §102 and §103 Rejections

Claims 31-34, 36-37, 39-47, 55-58 were rejected under 35 USC § 102(e) as anticipated by U.S. patent 5,831,335 to Miyamoto. Claims 31-35, 37-38, 42, 48, 50-54, 56-58 were rejected under 35 USC § 102(e) as anticipated by U.S. patent 5,525,543 to Chen. Applicant reserves the right to antedate either or both of these references under 37 CFR §1.131.

Both Miyamoto and Chen fabricate conductive layers in contact holes by means of chemical vapor deposition (CVD). The present Application discusses the shortcomings of this technique on page 2 lines 17-25, for example. Briefly, although CVD can obtain good step coverage for high-aspect holes, defects occur from unavoidable contamination during processing. Sputtering avoids contamination, but has problems of its own. Chen in fact gave up on sputtering because of its unacceptable coverage, illustrated in his Fig. 4.

The present invention avoids CVD's disadvantages while simultaneously improving the quality of sputter fabrication. As summarized on page 4 lines 17-19, Applicant's resputtering physically moves the initially deposited conductive material from the top and sides of the contact hole to its bottom surface. Comparing the initial deposits 150, 152, 154 of conductive material in Fig. 1A to the final conductive layers 354 and/or 356 in Figs. 3A and 3B shows that conductive material from the sidewalls has descended to fill in the corners of the bottom layer, making the bottom layer much more planar.

The CVD processes of Miyamoto and Chen—as well as conventional sputtering processes—cannot attain a structural configuration in which a planar conductive layer exists on the bottom of a contact hole, leaving its sidewall as an insulating material, substantially free of the conductive material.

Independent claim 31 distinguishes the structure of the present invention from those that could be achieved by either Miyamoto or Chen. For example, claim 31 recites that the vertical "sidewall" of the hole is an "insulating material." Further, the conductive layer on the bottom is clearly recited as covering "only" the bottom surface. Miyamoto shows the same layers forming both the sidewall and the bottom of the hole in his Fig. 3, the original insulator 2 now lying behind the sidewall. All of Chen's contact holes evince the same feature. The CVD processes employed in these references cannot deposit different materials at different locations within the

hole. Claims 32-37 depend from claim 31 and incorporate all of its recitations. Therefore, claims 31-37 define subject matter patentable over the references under both 35 USC §102 and §103.

Independent claim 39 distinguishes both Miyamoto and Chen in essentially the same way. The sidewall is an "insulating" material, without conductive properties. The planar layer on the bottom covers "only" the bottom surface. Claims 40-42 depend from claim 39, and distinguish the references in the same way.

Amended claim 43 distinguishes the references by reciting that the third material having a thickness variation less than 50% covers "only" the bottom surface. Claims 44-47 depend from claim 43.

Claim 48 follows claim 43, and additional recites that the third material has a "graded stoichiometry." The Office action states that Chen shows this feature in col. 4 lines 7-12. However, that passage teaches only a possible range of compositions that may occur among different devices using different process settings. Interpreting Chen's words to mean that different stoichiometries exist within different parts of a layer within the same device can only be done by impermissible hindsight from the present invention. There is no evidence that Chen intended any such meaning. Dependent claims 49-54 incorporate the features of claim 48, and add other distinguishing recitations as well. As to claim 49, Chen'd "high aspect ratio" cannot make up the deficiencies of Miyamoto; the combination still does not attain the other recitations of parent claim 48.

Claim 55 recites not only that the third material covers "only" the bottom surface as in the previous claims, but that "none of the third material" is present "in the sidewall." Claims 56-58 depend from claim 55.

Independent claim 59 is drawn to an integrated circuit having a contact hole having the properties recited in claim 31 as discussed above. Accordingly, claim 59 patentably distinguishes both Miyamoto and Chen for the same reasons. The cited Thomas patent adds nothing to the primary references except to show multiple contact holes in the same device, and

therefore the combination still does not reach the claim as amended. Claims 50-64 incorporate all the recitations of claim 59, and are patentable over any combination of the references for the same reasons.

Claim 65 recites an integrated circuit including at least one hole having the properties of claim 48, above. As in claim 65, combining Thomas adds nothing to the Miyamoto and Chen references. This claim and its dependent claims 66-70 still distinguish the references.

## CONCLUSION

Applicant respectfully urges that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6971 to facilitate prosecution of this Application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 24th day of January, 2002.

Amy Moriarty
Name

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Signature